CLAIMS

1. A method of forming an integrated circuit device comprising:

providing a semiconductor substrate;

forming a first patterned layer over the semiconductor substrate, wherein the first patterned layer has a first top, a first sidewall and a second sidewall and the first sidewall and the second sidewall are approximately vertical and opposite each other;

forming a second patterned layer over the patterned dielectric layer, wherein the second patterned layer has a second top, a third sidewall and a fourth sidewall, the third sidewall and the fourth sidewall are approximately vertical, opposite each other, and approximately co-planar with the first sidewall and the second sidewall, respectively;

forming an anti-reflective coating (ARC) over the second patterned layer;

forming a first dielectric layer over the first top and the second top and adjacent to the first sidewall, the second sidewall, the third sidewall, and the fourth sidewall;

removing a portion of the first dielectric layer, to form a first dielectric region adjacent the first sidewall and the third sidewall and a second dielectric region adjacent the third sidewall and the fourth sidewall, wherein the portion includes regions of the first dielectric layer formed over the first top and the second top;

removing the ARC after removing the portion of the first dielectric layer; and

forming a channel region within the semiconductor substrate under the first patterned layer and second patterned layer.

2. The method of claim 1, wherein the first patterned layer is a gate dielectric and the second patterned layer is a gate electrode.

3. The method of claim 2, further comprising forming shallow doped regions within the semiconductor substrate before removing the ARC.

4. The method of claim 2, wherein removing the ARC is a wet process.

5. The method of claim 2, wherein removing the ARC is a dry process.

6. The method of claim 2, further comprising:

forming a second dielectric layer over the first dielectric region and the second dielectric region;

forming a third dielectric layer over the second dielectric layer; and

anisotropically etching the third dielectric layer and the second dielectric layer to form first and second portions of spacers adjacent the first patterned layer and second patterned layer.

7. The method of claim 6, further comprising:

forming a fourth layer over the third dielectric layer; and

anisotropically etching the fourth layer selective to the third dielectric layer.

8. The method of claim 7, wherein anisotropically etching the fourth layer forms a third portion of the spacers.

9. The method of claim 8, wherein the fourth layer is an oxide.

10. The method of claim 7, further comprising:
forming a silicide region over the first patterned layer;
removing the fourth layer after anisotropically etching the fourth layer and before forming the silicide.

11. The method of claim 10, wherein the fourth layer is amorphous silicon.

12. The method of claim 6, wherein the second dielectric layer is an oxide and the third dielectric layer is a nitride.

13. The method of claim 1, wherein the first dielectric region and the second dielectric region comprise a stack of a first oxide layer and a first nitride layer formed over the first oxide layer.

14. The method of claim 13, further comprising a second oxide layer.

15. The method of claim 1, further comprising oxidizing the first and second dielectric regions before removing the portion of the ARC, wherein removing the ARC is a wet process.

16. The method of claim 1, wherein the second patterned layer is a charge storage layer of a non-volatile memory device.

17. A method of forming an integrated circuit device comprising:

providing a semiconductor substrate;

forming a patterned dielectric layer over the semiconductor substrate,

forming a patterned conductive layer over the patterned dielectric layer;

forming an anti-reflective coating (ARC) over the patterned conductive layer;

forming a first dielectric layer over the patterned dielectric layer and the patterned conductive layer;

forming a second dielectric layer over the first dielectric layer;

forming a first layer over the second dielectric layer;

removing portions of the first layer to form a first patterned layer, wherein the first patterned layer is adjacent the patterned conductive layer and the patterned dielectric layer;

removing portions of the second dielectric to form first dielectric regions adjacent the first patterned layer;

removing portions of the first dielectric to form second dielectric regions adjacent the first dielectric regions; and

removing the ARC after removing the portions of the first dielectric layer

18. The method of claim 17, further comprising:

forming a second layer over the first layer;

removing a portion of the second layer selective to the first layer to form patterned first portions of the second layer adjacent to the first patterned layer .

19. The method of claim 18, wherein removing the ARC is a dry process.

20. The method of claim 18, wherein the second layer is an oxide, the first layer is a nitride, the second dielectric layer is an oxide, and the first dielectric layer is an oxide.

21. The method of claim 20, further comprising removing the portions of the second layer, wherein the second layer is amorphous silicon.

22. The method of claim 17, wherein the first dielectric layer is an oxide, the second dielectric layer is a nitride and the first layer is an oxide.

23. The method of claim 22, wherein removing the ARC is a wet process.

24. A method of forming an integrated circuit device comprising:

providing a semiconductor substrate having a first portion and a second portion;

forming a gate stack comprising:

a gate dielectric formed over the first portion of the semiconductor substrate; and

a gate electrode formed over the gate dielectric;

forming a first patterned anti-reflective coating (ARC) over the gate stack;

forming a non-volatile memory stack comprising:

a charge storage layer formed over the second portion of the semiconductor substrate; and

a first dielectric layer formed over the charge storage layer;

forming a second patterned ARC over the non-volatile memory stack;

forming a second dielectric layer over the gate stack and the non-volatile memory stack;

removing portions of the second dielectric layer to form first spacers adjacent the gate stack and the non-volatile memory stack;

removing the first patterned ARC and the second patterned ARC after removing portions of the second dielectric layer;

forming a first channel under the gate stack; and

forming a second channel under the non-volatile memory stack.

25. The method of claim 24, further comprising:

forming a third dielectric layer over first spacers;

forming a fourth dielectric layer over the third dielectric layer;

removing portions of the third dielectric layer to form second spacers adjacent the first spacers; and

removing portions of the fourth dielectric layer to form third spacers adjacent the second spacers.

26. The method of claim 25, wherein removing the first patterned ARC and the second patterned ARC is before forming a third dielectric layer and forming a fourth dielectric layer.

27. The method of claim 26, wherein the second dielectric layer is densified prior to forming first spacers and removing the first patterned ARC and the second patterned ARC is a wet process.

28. The method of claim 27, wherein the second dielectric layer is an oxide, the third dielectric layer is an oxide, and the fourth dielectric layer is a nitride.

29. An integrated circuit device comprising:

a semiconductor substrate;

a stack comprising:

a patterned dielectric layer formed over the semiconductor substrate;

a patterned conductive layer formed over the patterned dielectric layer;

a first sidewall; and

a second sidewall, wherein the second sidewall is adjacent the first sidewall;

a first electrode region within the semiconductor substrate and adjacent the first sidewall;

a second electrode region within the semiconductor substrate and adjacent the second sidewall;

a channel region between the first electrode region and the second electrode region and under the stack;

oxide spacers adjacent the first sidewall and the second sidewall, wherein the oxide spacers have a first height; and

nitride spacers adjacent the first oxide spacers, wherein the nitride spacers have a second height which is less than the first height.

30. An integrated circuit device comprising:

a semiconductor substrate having a top surface;

a stack formed on the semiconductor substrate comprising:

a first layer;

a second layer formed over the first layer;

a first sidewall; and

a second sidewall opposite the first sidewall;

spacers adjacent the first sidewall and the second sidewall, wherein a first portion of the top surface of the semiconductor substrate is under the spacers, a second portion is under the stack, and the first portion is substantially co-planar with the second portion;

a first doped region within the semiconductor substrate and adjacent the first sidewall;

a second doped region within the semiconductor substrate and adjacent the second sidewall; and

a channel region between the first doped region and the second doped region and within the semiconductor substrate.

31. The integrated circuit device of claim 30, wherein a first portion of the first and doped region and a second portion of the second doped region are under the gate dielectric.